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SIRFN Power System Testing

Inter-area Oscillation Damping in a Scaled Version of the Kundur's Two Area Power System

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Motivation

The increasing deployment of new technologies to contribute to the decarbonization of power systems is imposing new challenges in terms of system dynamics and stability. To deal with different operating and control issues in this sense, and support actual needs, advanced tools and solutions are required. Therefore, this poster presents a two-stage approach to test and validate controller structures to damp inter-area oscillations, developed within the ISGAN SIRFN PST subtask: Stability of Low-inertia transmission interconnections [1].

First, the previously developed digital twin (DT) [2] was validated with laboratory measurements to ensure that the deviations from the Dynamic hardware emulator of an electric power system (DHEPS) [3] are acceptable. To assess the accuracy of the DT and quantify the errors, static and dynamic comparisons were made between laboratory measurements and the simulation model. With the DT of the DHEPS and a real-time simulator, it is possible to test and improve a digital controller for damping inter-area oscillations in a controller hardware in the loop (CHIL) scheme. In the second step, the controller was connected directly to the DHEPS and tested in a physical environment. It is shown that with a conventional power system stabilizer (PSS) and a proportional wide-area damping controller (WADC), the damping of inter-area oscillations is improved in an emulated power system environment. In addition, with the lab setup created, different types of controllers and other challenges related to existing and new stability phenomena [4,5,6] or issues arising from cyber-physical interactions through increasingly digitalized control technologies can be investigated.

Inter-area oscillation damping via CHIL and DHEPS setups

To test and investigate the proposed controller, a CHIL setup was created as shown in figure 1, where the DT is simulated on an OPAL-RT real-time simulator, and the terminal voltages of generator 11 and generator 21 are sent to the PMUs via an analogue signal. In addition, the voltage signals are downscaled in amplitude by a factor of 100 so that OPAL-RT's analogue output cards are used instead of the integrated amplifier. PMUs estimate the voltage phasors of the analogue sinusoidal signals, while the RPi, which is used as a digital controller, reads and processes them. The processed signals are sent back as analogue signals to the OPAL-RT and thus to the running real-time simulation of the digital twin, closing the loop.
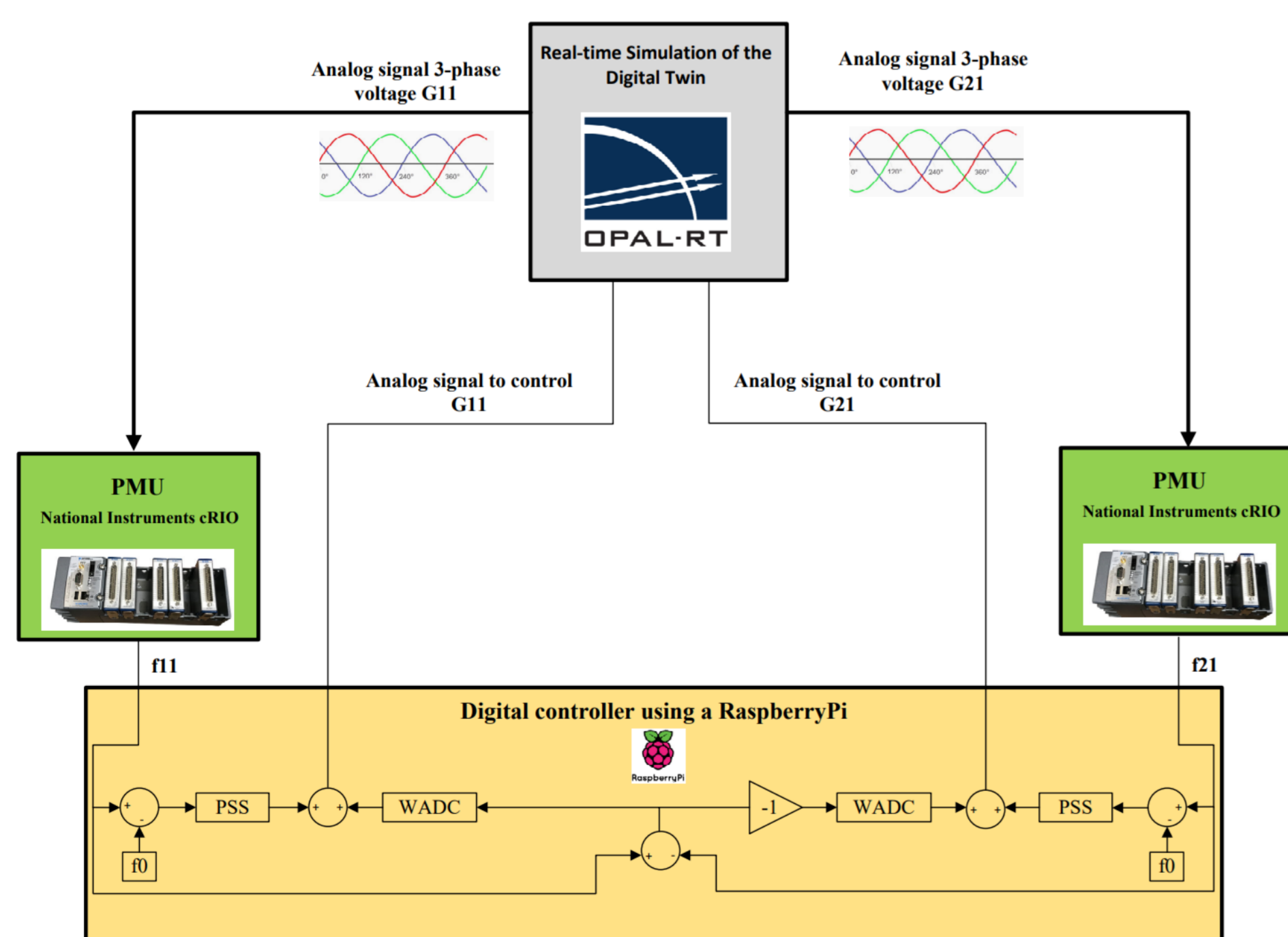

Figure 1 - Schematic drawing of the CHIL setup

After the successful implementation of the controller in the CHIL setup, the controller is transferred to the DHEPS, and the setup is shown in figure 2, whereby the operating principle is very similar to the CHIL setup, with the difference, that the analogue signals are connected to the ABB Unitrols where they are added to the AVR's input signals.
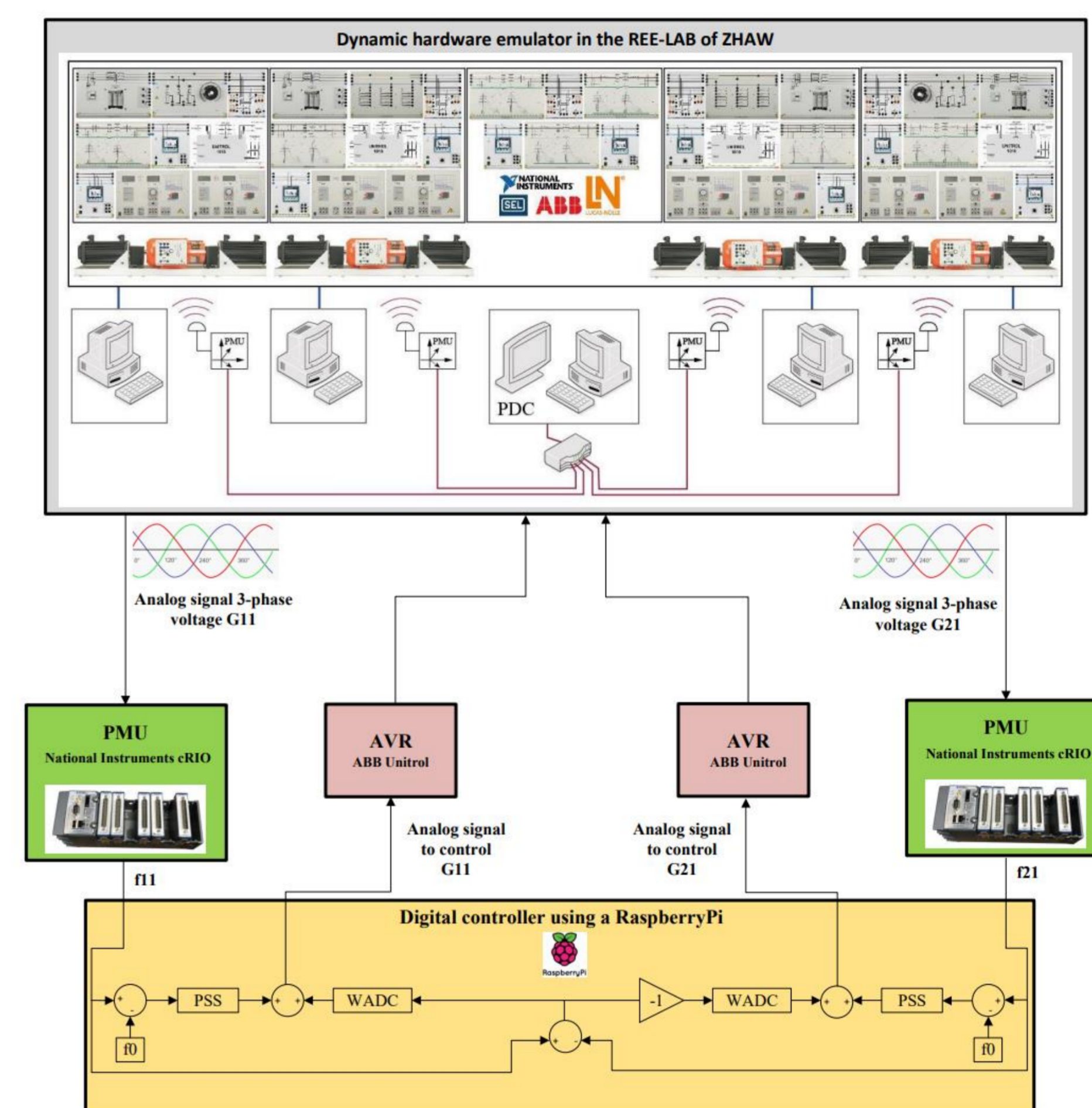

Figure 2 - Schematic drawing of the DHEPS setup

Results:

Figure 3 displays the frequency deviation between the areas to demonstrate the effectiveness of the implemented controllers in damping inter-area oscillations. In order to quantitatively assess the system performance in terms of inter-area oscillation damping, the stability index was calculated for the frequency deviation between the areas according to the following equation:

$$S = \sum_{t=0}^{t_{end}} |f(t) - f(t-1)| \cdot t$$

The numerical results are provided in the tables included, where the performance indexes are normalized so that the case without control has a value of 1.

	Performance index
Without control	1
PSS only	0.46
PSS / WADC	0.28

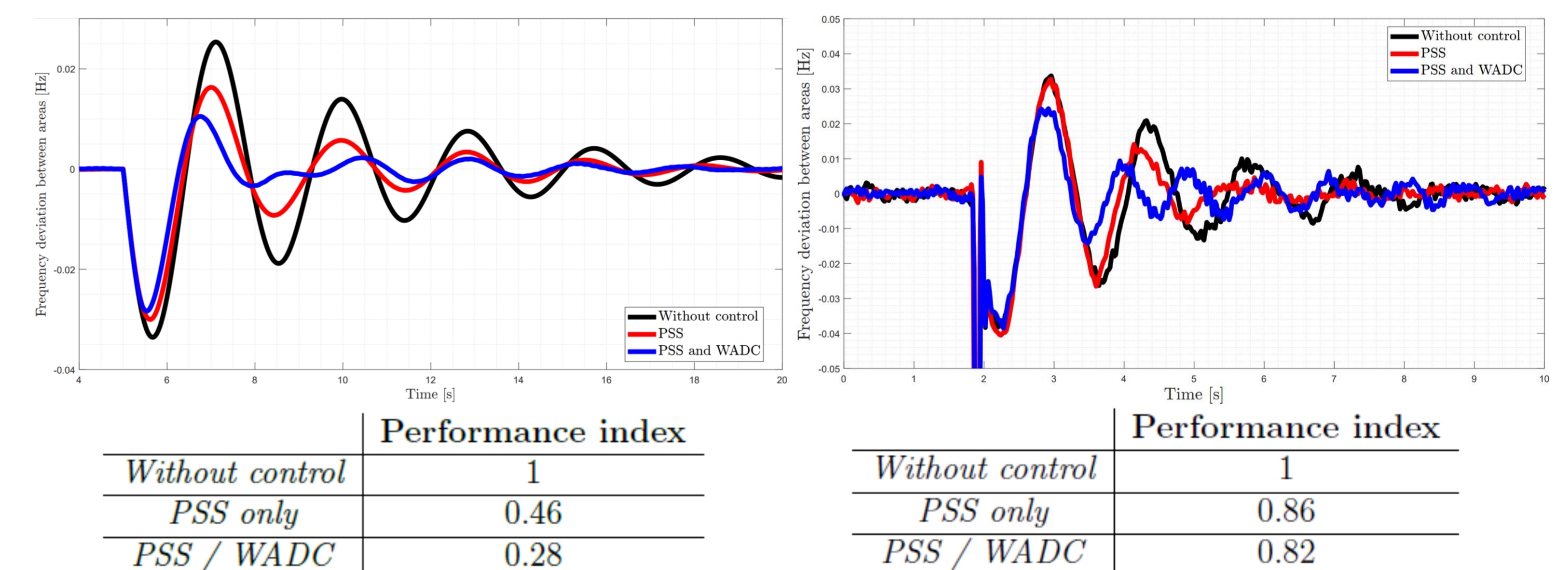|	Performance index
Without control	1
PSS only	0.86
PSS / WADC	0.82

Figure 3 - Frequency deviation for the three cases (without control, PSS only, PSS and WADC) after the tie-line trip within the digital twin setup (left) and with the dynamic hardware emulator (right)

Conclusion

It can be concluded that a very simple proportional structure of the WADC can in fact provide additional damping to the inter-area modes observed with the DHEPS. However, it should be noted that the control signals affect the terminal voltage and therefore the voltage should be monitored to ensure that no limits are violated. If a tuning approach is used, it is certainly advantageous to consider a constraint on the voltage limits.

Working with real devices such as measurement devices, digital controllers, and the dynamic hardware emulator, has generally been challenging as the signal noise involved is sometimes difficult to handle. In addition, establishing communication links among the considered devices is often difficult, as communication can be interrupted for no apparent reason.

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