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# Laboratory Implementation of a Wide-area Damping Controller using a Dynamic Hardware Emulator Sandro Kellermüller \* Miguel Ramirez-Gonzalez \* Artjoms Obushevs \* Petr Korba \*

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**Abstract:** The ongoing decarbonisation of the electric power system brings new challenges in terms of system dynamics and stability, as the substitution of generation units with rotating masses towards generation units based on power electronics entails a substantial loss of inertia. To meet the new challenges and maintain the reliability of the electrical grid, innovative solutions are required. Therefore, this paper presents a two-step approach to test and validate controller structures for damping inter-area oscillations. First, the controller was developed and tested in a control hardware in the loop environment. Then, the controller was transferred to a dynamic hardware emulator (scaled version of the Kundur's two area transmission network in the laboratory consisting of physical hardware) for final performance validation. It is shown that with a conventional power system stabilizer (PSS) and a proportional wide-area damping controller (WADC), the damping of inter-area oscillations is improved in an emulated power system. In addition, with the setup created, different types of controllers and other challenges related to wide-area damping control can be investigated in the future.

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*Keywords:* Inter-area oscillations, Wide-area Damping Controller (WADC), Dynamic Hardware Emulator, Control Hardware in the Loop (CHIL), Phasor Measurement Unit (PMU)

# 1. INTRODUCTION

With the continuing trend towards fossil-free energy production in Europe, as well as the increasing energy consumption due to more electrical consumers such as electric cars or heat pumps, the characteristics of the grid are changing significantly. The large-scale integration of nonsynchronous generation reduces the overall inertia of the system and impacts its dynamic properties. In addition, the increasing consumption and new regulations [ACER (2021)] are pushing the existing transmission lines to their physical limits. Furthermore, the size and complexity of power systems are continuously growing due to the synchronization with more networks. For example, the Continental European Energy System was synchronized with Turkey in 2010 [Nassar and Weber (2012)] and with Ukraine and Moldova in 2022 [ENTSO-E (2022a)]. Moreover, synchronisation with the Baltic countries (Latvia, Lithuania, Estonia) is being planned in 2025 [ENTSO-E] (2022b)]. Although very large transmission networks can provide a more efficient use of resources, and increased robustness and reliability, they are more complex to coordinate and operate. In addition, the delivery of power over long transmission lines may potentially give place to the development of critical inter-area oscillations. In December 2016 [System Protection and Dynamics Working Group ENTSO-E (2018)] and 2017 [System Protection and Dynamics Working Group ENTSO-E (2017)], a related scenario occurred and appropriate measures had to be taken to ensure stability. As a consequence of the event in 2017, ENTSO-E requires additional innovative damping solutions and devices to minimise severe consequences of inter-area oscillations [System Protection and Dynamics Working Group ENTSO-E (2017)]. Taking into account the aforementioned statements and trends, damping interarea oscillations is of great interest within the transmission system operators (TSOs), especially in large power grids such as the Continental European synchronous area.

Although power system stabilizers (PSSs) have been commonly used to mitigate power system oscillations through generator excitation systems [Stativă et al. (2012), Dobrowolski et al. (2018)], the use of local signals for supplementary control in this sense may lead to ineffective damping of inter-area modes. However, the deployment of more and more PMUs in power systems [Derviskadic (2022)] has opened the possibility to implement advanced schemes known as Wide-Area Damping Controllers (WADC), which are based on the use of synchronized measurements at strategic locations. A broad variety of devices can be used as actuators for WADCs, such as synchronous machines, HVDC links [Pierre et al. (2019)] or flexible AC transmission systems (FACTS) devices [Yao et al. (2014)].

There are many studies in the literature dedicated to the damping of inter-area oscillations with WADC structures. However, these have almost exclusively been carried out with dynamic simulations without including any hardware. There are only a few studies in which real measur-

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Fig. 1. Single line diagram of the dynamic hardware emulator.

ing devices or controllers are used in a hardware-in-theloop approach [Sevilla et al. (2021), Rebello et al. (2021), Zhang et al. (2021)], but none of them are based solely on hardware. To close this gap, this paper proposes a WADC in a purely hardware environment using a dynamic hardware emulator of a transmission system in the laboratory [Baltensperger et al. (2020)]. It is clear that to ensure the practical application and effectiveness of WADC solutions, controller testing and evaluation under realistic conditions (or close to reality) is inevitably required. Therefore, the work presented here takes a step forward for the development and implementation of controller prototypes under practical operational uncertainties such as time delays, noise, communication issues, etc., which may affect control robustness and performance. Based on this approach, a controller hardware in the loop (CHIL) setup was built first to design and test the proposed controller. After positive evaluation on this setup, the controller was then transferred and successfully integrated into the dynamic hardware emulator for final testing and practical assessment.

# 2. CONTROLLER HARDWARE IN THE LOOP SETUP

In order to design the controller and determine the appropriate parameters, a CHIL setup was first realised to ensure that no hardware would break on the dynamic hardware emulator during the test with the real equipment. The required digital twin of the dynamic hardware emulator has been developed in [Kellermüller (2022)] and the single line diagram is visualised in figure 1. Compared to [Baltensperger et al. (2020)], the dynamic hardware emulator has been slightly modified, with the length of the transmission lines connecting the two areas increased from 300km to 600km. An overview of the complete CHIL setup is shown in figure 2 where the digital twin is simulated on an OPAL-RT realtime simulator and the terminal voltages of generator 11 and generator 21 are sent to the PMUs via an analogue signal. In addition, the voltage signals are downscaled in amplitude by a factor of 100 so that OPAL-RT's analogue output cards can be used instead of the integrated amplifier. This does not cause any problems because the down scaling of the amplitude does not affect the frequency of the signal. Then, the PMUs estimate the voltage phasors of the analogue sinusoidal signals and the Raspberry Pi, which is used as a digital controller, reads and processes them. Since the Raspberry Pi itself does not have the capability to generate analogue signals, the device was expanded with the so-called Raspberry Pi High-Precision AD/DA Expansion Board. With this expansion



Fig. 2. Scheme of the implemented CHIL setup.

board, two additional analogue output channels and four analogue input channels are available. In the setup considered here, only the analogue outputs are used, and the output voltage on each channel can be set independently between 0V and 5V. Finally, the processed signals are sent back as analogue signals to the OPAL-RT and thus to the running real-time simulation of the digital twin, closing the loop. To be able to read the measurements of the PMUs, a communication link has to be established. For this purpose, there is a python package called PyMU that works as a client/server relationship, where the PMU is the server and the Raspberry Pi is the client which asks for measurements. Within this package, it is possible to read the PMU measurements in real time (full documentation is available in [Drew (2016)]). In addition, a separate client object must be created in Python for each PMU in order to be able to read out measurements from several PMUs.

# 2.1 Controller structure

As depicted in figure 2, the proposed controller structure consists of a PSS and a WADC. In this study the so called conventional PSS (CPSS) has been chosen as depicted in figure 3, where the locally measured frequency deviation  $\Delta f$  is the input. In addition,  $\Delta f$  is pre-filtered with a lowpass filter to obtain a smooth signal. The CPSS consists of a washout filter, a proportional gain, two lead/lag elements and an output limiter. Both lead/lag elements here have the same time constants  $(T_1 \text{ and } T_2)$ , which is generally not the case. Finally, maximum and minimum limits are defined before the signal is passed on to the automatic voltage regulator (AVR) of the synchronous machine. Finally, the CPSS is complemented with a WADC, which is shown in figure 4. The frequency of the generator G11 in area 1 is subtracted from the one of generator G21 in area 2 and then multiplied with a simple proportional gain. Besides the measurement noise contained in the PMU stream, there is an additional problem that occurs immediately after a disturbance (line trip, sudden load change, etc.), where a sharp peak can be observed, as shown in figure 5 (blue). If this peak is not filtered, the controller would react strongly and instabilities could occur. The first-order low-pass filter included in figure 3 is not able to suppress these spikes, so an alternative solution is needed. In this case the issue has been solved with the application



Fig. 3. Block diagram of the low-pass filter and the CPSS.



Fig. 4. Block diagram of the WADC.



Fig. 5. Measurement issue of the PMUs after a disturbance and the corresponding filtered signal.

of a derivative filter, which is described in the following equation:

$$f(k) = \begin{cases} f(k-1), & \text{if } \frac{df(k)}{dt} > l\\ f(k), & \text{otherwise} \end{cases}$$
(1)

where f(k) and f(k-1) are respectively the frequency samples at time instant k and k-1, and l is the predefined threshold. If the derivative of f(k) exceeds the threshold l, f(k) is skipped and the previous sample f(k-1) is taken instead. The black curve in figure 5 illustrates the resultant signal after being filtered with the derivative filter, where it can be observed that just the spike is removed and the rest of the signal is not manipulated. The benefit of using such a filter is that no delay is introduced compared to a conventional low-pass filter for example. It is assumed that these spikes are related to phase jumps in the AC signal, which are then reflected from the phasor estimation algorithm of the PMU as spikes in the frequency [Roscoe et al. (2017)]. Therefore, they can be removed without any doubts of neglecting any important dynamic phenomena.

# 2.2 Parameter tuning of the controller

Many different methods for tuning the PSS are described in the literature, both model-based methods and methods that do not require a model of the power system. In the model-free approaches, optimisation algorithms are used within an iterative process to derive the optimal parameters. For this work, iterative tuning of the PSS is challenging because the model for the CHIL setup needs to be recompiled frequently, which is very time consuming. Another problem is the high frequency signal noise of the frequency, because for certain time constants  $T_1$  and  $T_2$  the amplitudes of the high frequencies are amplified and thus the controller does not work as planned. This phenomenon can be well explained with the Bode plots in figure 6. The two Bode plots show different configurations in terms of the time constants  $T_1$  and  $T_2$ , the gain is set to one in both cases and the time constant of the low-pass filter is set to  $T_f = 0.04$  for both cases. In addition, the Nyquist frequency is marked in figure 6, which is half of the sampling frequency ( $\omega_N = 78.54 \ rad$ ). According to the Nyquist-Shannon sampling theorem, a sampled signal does not contain frequencies above the Nyquist frequency. This means that the high-frequency noise contained in the input signal of the CPSS must be lower than the Nyquist frequency, but still in a similar frequency range. In a typical time constant configuration, represented by the black curve in the top diagram of figure 6, the noise around the Nyquist frequency is greatly amplified and the controller does not work. When the gain of the CPSS is increased, the problem becomes even worse. Furthermore, the time constant of the low-pass filter could be increased, but this would involve a massive loss of phase, as the time constant  $T_f$  would have to be increased significantly. For the determination of the final time constants, Bode plots of different combinations of  $T_1$  and  $T_2$  were made and compared with each other. In addition, some of the combinations were tested experimentally in the CHIL setup and analysed. Under the above considerations, practical values for time constants  $T_1$  and  $T_2$  were determined to be within a very small range for the proposed control configuration, consequently leading to the selection of the time constants associated with the red curve in figure 6. After that, and with the help of several simulations in the CHIL-setup, the gain  $K_{PSS}$  was increased step by step until the noise of the signal was amplified so much that the function of the controller was no longer as desired. Taking this threshold and an additional margin into account, the gain was set. The sampling time  $T_s$  was set to 0.04 seconds, which means that every second sample is taken from the PMU. Furthermore, the time constant  $T_w$  of the washout filter was set to 10 seconds, as this parameter is not critical [Kundur (1994)] and thus no further investigation is needed. Since the WADC consists of only one gain, the tuning of  $K_{WADC}$ was also done empirically in the same way as the gain of the CPSS. A summary of the chosen parameters in the CHIL setup are listed in table 1. Finally, the controller was discretized with Tustin's method and implemented on the digital controller.

#### 2.3 Simulation setting and results

To provoke the development of inter-area oscillations, the system was disturbed with the disconnection of one of the



Fig. 6. Bode plot of two different PSS configurations including the low-pass filter.

Table 1. Parameters of the CPSS and WADC used for the HIL setup.

Parameter	Value
$T_{f}$	0.08
$T_w$	10
$T_1$	0.1
$T_2$	0.05
$K_{PSS}$	120
$K_{WADC}$	40

tie lines between the areas, in a case study where 310 W were transferred from Area 1 to Area 2. Three different scenarios were carried out and compared with each other. The first scenario does not integrate an additional controller, whereas the second and third scenarios use respectively a PSS and a combination of PSS and WADC. A quantitative evaluation of the damping was carried out by means of a performance index as in equation 2, where two consecutive samples of a signal are subtracted from each other and multiplied by the time t. The time t = 0 is the time of the disturbance in each case, which has the consequence that differences between samples are weighted more heavily long after the disturbance.

$$S = \sum_{t=0}^{t_{end}} |f(t) - f(t-1)| \cdot t$$
 (2)

To demonstrate the effectiveness of the proposed controller in damping inter-area oscillation, the frequency deviation between the areas for the three scenarios is plotted in figure 7 and the corresponding performance indexes are listed in table 2. Note that the performance indexes are normalized so that the scenario without a controller has the value 1. It can be observed that the performance index can be drastically reduced with the PSS and further improvements can be achieved with the PSS/WADC combination. Furthermore, with the controllers used, the oscillating active power flow (see figure 8) from area 1 to area 2 can be more effectively damped.

> Table 2. Normalized performance index of the three scenarios after the tie line trip based on the frequency deviations between the areas in the CHIL setup.

Performance index	Value
Without control	1
PSS	0.52
PSS and WADC	0.26



Fig. 7. Frequency deviation between area 1 and area 2 for the three scenarios after the tie line trip within the CHIL setup.



Fig. 8. Active power transfer over the tie line of the three scenarios within the CHIL setup after the tie line trip.



Fig. 9. Schematic drawing of the dynamic hardware emulator test bench including the dynamic hardware emulator itself, PMUs, the ABB Unitrols and the digital controller.

#### 3. DYNAMIC HARDWARE EMULATOR SETUP

After the successful implementation of the controller in the CHIL setup, the controller is transferred to the dynamic hardware emulator. A schematic drawing of the setup is visualised in figure 9, where the operating principle is very similar to that of the CHIL setup. Instead of simulating the digital twin, the dynamic hardware emulator is used and the PMUs physically measure the phasors of the terminal voltages of the synchronous generators 11/21, and the Raspberry Pi used as digital controller reads and processes the measurements. Finally, the control signal from the controller is transferred to the Unitrol as an analogue signal, where it is added to the AVR's input.



Fig. 10. Bode plot of the CPSS with one and two lead/lag elements.

#### 3.1 Controller structure and parameter tuning

The problem of measurement noise accompanying the CPSS has already been discussed in the section 2.2. When using the dynamic hardware emulator, the problem is exacerbated because not only the measurement noise but also additional frequency fluctuations are contained in the signal. These additional fluctuations are due to the small size and correspondingly low weight of the synchronous generators in the laboratory. Even when the rotor inertia is artificially increased, the fluctuations do not disappear. Consequently, in the structure of the CPSS shown in figure 3, the controller did not work initially because the high frequencies were amplified even when the time constants of the lead/lag links were set to  $T_1 = 0.1$  and  $T_2 = 0.05$ . To solve this problem, one lead/lag element was removed. The corresponding Bode plot compared to the case with two lead/lag elements is shown in figure 10, where it can be seen that frequencies around the Nyquist frequency are no longer amplified and the controller works properly. Finally, the table 3 shows the set of parameters for the CPSS and the WADC in the dynamic hardware emulator, where the gains were again empirically tuned.

Table 3. Parameters of the CPSS and WADC used in the dynamic hardware emulator setup.

Parameter	Value
$T_{f}$	0.04
$T_w$	10
$T_1$	0.1
$T_2$	0.05
$K_{PSS}$	60
$K_{WADC}$	50

#### 3.2 Experimental setting and results

Again, the same three scenarios (without additional control loop, conventional PSS only, and PSS combined with WADC) have been investigated and compared to each other, whereas the disturbance remains also unchanged (trip of one of the tie lines). Similar conditions as in the CHIL setup in terms of loading were applied and the transferred active power from area 1 to area 2 is around 320W. The resulting frequency deviations between the areas are shown in figure 11 for each scenario, where the effect of the proposed controller is clearly visible as the oscillations decay much faster in the controlled scenarios.



Fig. 11. Frequency deviation between area 1 and area 2 for the three scenarios after the tie line trip within the dynamic hardware emulator setup.

> Table 4. Normalized performance index of the three scenarios after the tie line trip based on the frequency deviations between the areas in the dynamic hardware emulator setup.

Performance index	Value
Without control	1
$\mathbf{PSS}$	0.88
PSS and WADC	0.79

To further strengthen the value of the proposed controller, the performance index is calculated according to equation 2 and the obtained values are listed in table 4, where it is clear that the index decreases with the integration of the PSS as well as the WADC and PSS combination.

#### 4. CONCLUSION

In this study, a two-stage approach was followed to develop a damping control strategy for inter-area oscillations using an available dynamic hardware emulator in the laboratory. The proposed digital controller was tested and improved in the CHIL setup and subsequently implemented in an emulated power system environment. According to the obtained results, improvements in the damping of the interarea oscillations were visible and measurable when only the conventional PSS was used. Furthermore, this damping was additionally increased by using the proportional wide-area damping controller. As seen with the dynamic hardware emulator, a very simple proportional structure of the WADC can already provide additional damping of the inter-area modes.

Future research activities are planned to take communication issues into account, such as delay in the signals as in [Zhang et al. (2021)] or the loss of time synchronization in PMU based applications and its impact on system stability [Almas and Vanfretti (2016)]. In addition, more complex controller structures in terms of damping inter-area oscillations will be investigated, for example those discussed in [Sevilla et al. (2021)]. During exploration of the digital twin and the dynamic hardware emulator, it has been noticed that the electromechanical oscillations in general are small and thus the tie line connecting the two areas has been extended to 600km. In order to reduce the damping, the ohmic loads (constant impedance) can be substituted with loads of constant power, which is demonstrated in [Peng and Nair (2009)].

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